
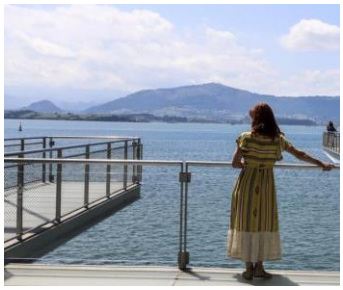

1st Workshop of Spanish Chip Chairs

25th November 2025, Santander, Spain

CALL FOR PARTICIPATION

As described on the website of the Ministry of Economic Affairs and Digital Transformation[1], this ministry, through the Secretary of State for Telecommunications and Digital Infrastructure, launched a call for proposals in 2023 to finance, with funds from the European Recovery and Resilience Facility, the creation of University-Business Chairs for the period 2023-2027, whose activity would focus on research, dissemination, and training in the different application areas of microelectronics. The Program was part of the Strategic Project for Economic Recovery and Transformation (PERTE), called "PERTE Chip," a strategic initiative aimed at developing the scientific, design, and production capabilities of the Spanish microelectronics and semiconductor industry. As part of this project, the 17 Chip Chairs, approved and funded since July 2024, have been working to achieve their research, training, and dissemination objectives in close collaboration with the companies under their respective sponsorships.

The Design of Circuits and Integrated Systems (DCIS) conference is a well-established international meeting that, for over 40 years, has provided opportunities for both academic researchers and industry professionals to exchange new ideas and application experiences in the highly active fields of micro and nanoelectronic circuits and integrated systems. Given the significant national participation, it is a meeting point for a large part of the Spanish microelectronics community. This year, the conference will take place in Santander, from November 26 to 28.

The 1st Chip Chair Seminar aims to serve as a meeting point for the Chairs after its first year and a half of operation. A forum to showcase the most significant scientific and technological goals achieved to date, share future plans, facilitate the exchange of experiences, and enhance opportunities for collaboration.

Interested Chairs should submit a three pages abstract of their presentations describing the most relevant achievements in their research and training activities. A template will be available at the workshop web page.

Important Dates

Deadline for submission: June 8th, 2025
Notification of acceptance: July 20th, 2025
Deadline for final paper submission: September 7th, 2025
Registration open: July 20th, 2025

Co-located with: DCIS 2025 SANTANDER

Organizer
Eugenio Villar (Cátedra Chip Cantabria)

Steering Board
Antonio Acosta (Cátedra Chip USECHIP)
Armando Astarloa (Cátedra Chip SoC4sensing UPV/EHU)
Francisco Ballester (Cátedra UPV-VaSiC de Diseño Microelectrónico)
Guillermo Carpintero (Cátedra Chip EPICPack)
Francisco Diaz (Cátedra NextChiP)
Cristina de Dios (Cátedra EPIQ UC3M – Arquimea Research Center)
Francisco Gamiz (Cátedra +QCHIP-UGR)
Paula López (Cátedra Televés de Microelectrónica)
Juan Carlos López (Cátedra PERTE Chip UCLM)
Marisa López-Vallejo (Cátedra UPM-Indra en Microelectrónica)
Enrique Márquez-Segura (Cátedra Chip Málaga Microelectronics)
Pascual Muñoz (Cátedra Chip Fotónico PIC-UPV)
Candid Reig (Cátedra PERTE Chip UV en Semiconductores)
Antonio Rubio (Cátedra PERTE Chip UPC)
Eugenio Villar (Cátedra Chip Cantabria)

International Liaisons
Marco Demicheli (Chips-IT)
Wolfgang Nebel (Chips Design Germany)

Venue

DCIS 2025 will be held at Hotel Santemar,
Joaquin Costa, 28. 39005 Santander, Spain
Hotel.santemar@hsantos.es +34 942272900

Web page: dcis2025.unican.es

Organized by: UC C3 Cantabria Chip Chair

Supported by: Financiado por la Unión Europea NextGenerationEU; Gobierno de España; Ministerio para la Transformación Digital y de la Función Pública; Plan de Recuperación, Transformación y Resiliencia; España digital; PERTE Chip; ACORDE

Contact: c3_secretaria@unican.es

[1] https://portalayudas.digital.gob.es/catedras-chip/Paginas/Index.aspx